AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A semiconductor integrated circuit, comprising:

a plurality of layers provided on a semiconductor substrate;

wires provided in a first layer that is one of said plurality of layers, said wires excluding those having a wire width wider than a predetermined wire width; and

wire dummies provided in a second layer different from the first layer by avoiding areas that are directly above or below positions of said wires provided in said first layer.

Claim 2 (Original): The semiconductor integrated circuit as claimed in claim 1, wherein the first layer is a layer immediately above or immediately below the second layer.

Claim 3 (Original): The semiconductor integrated circuit as claimed in claim 1, wherein said wires are signal wires excluding power supply wires.

Claim 4 (Currently Amended): A semiconductor integrated circuit, comprising:

a plurality of layers provided on a semiconductor substrate;

signal wires and power supply lines are provided in a first layer that is one of said plurality of layers; and

wire dummies provided in a second layer different from the first layer and having an arrangement that avoids areas overlapping positions of said signal wires,

wherein ~~said wires are signal wires excluding power supply wires, and~~

said wire dummies are further provided in areas overlapping positions of said power supply wires that are provided in the first layer.

Claim 5 (Currently Amended): A semiconductor integrated circuit, comprising:

a plurality of layers provided on a semiconductor substrate;

signal wires and power supply wires are provided in a first layer that is one of said plurality of layers; and

wire dummies provided in a second layer different from the first layer and having an arrangement that avoids areas overlapping positions of said signal wires,

wherein ~~said wires are signal wires excluding power supply wires,~~

said wire dummies are further provided in areas overlapping positions of said power supply wires that are provided in the first layer, and

said signal wires have a width less than a predetermined wire width, and said power supply wires have a width greater than the predetermined wire width.

Claim 6 (Previously Presented): The semiconductor integrated circuit as claimed in claim 1, wherein said wire dummies further avoid areas that are directly above positions of polysilicon or diffusion layers.

Claim 7 (Canceled).

Claim 8 (Currently Amended): A semiconductor integrated circuit, comprising:

a wire layer;

wires provided in said wire layer; and

square dummy patterns provided in said wire layer and having different sizes,

wherein ~~said square dummy patterns having different sizes are arranged at respective different pattern intervals~~ the size of one of said square dummy patterns that is arranged between two adjacent wires of said wires spaced apart from each other by a first distance is larger than the size of one of said

dummy patterns that is arranged between two adjacent wires of said wires spaced apart from each other by a second distance that is shorter than the first distance.

Claim 9 (Canceled).

Claim 10 (Original): A semiconductor integrated circuit, comprising:

a plurality of wire layers stacked one over another;

a plurality of wires including first wires and second wires and arranged in a first wire layer that is one of said wire layers, said plurality of wires being arranged at various intervals, a shortest of which is a predetermined interval, said first wires having wires on both sides thereof at a distance equal to said predetermined interval, and said second wires having no wires on both sides thereof at a distance equal to the predetermined interval; and

dummy patterns provided in a second wire layer immediately above or below the first wire layer, said dummy patterns being arranged in areas overlapping positions of said first wires and being absent in areas overlapping positions of said second wires.

Claim 11 (Original): The semiconductor integrated circuit as claimed in claim 10, wherein said plurality of wires includes third wires having a wire only on one side thereof at a distance equal to the predetermined interval, and said dummy patterns are arranged in the second layer in areas overlapping positions of said third wires.

Claim 12 (Original): The semiconductor integrated circuit as claimed in claim 10, wherein said plurality of wires includes third wires having a wire only on one side thereof at a distance equal to the predetermined interval, and said dummy patterns are absent in the second layer in areas overlapping positions of said third wires.

Claim 13 (Original): A semiconductor integrated circuit, comprising:

a plurality of wire layers stacked one over another;

a plurality of wires including first wires, second wires, and third wires, and arranged in a first wire layer that is one of said wire layers, said first wires being narrower than a predetermined width, said second wires being equal to or wider than the predetermined width and carrying a power supply potential, and said third wires being equal to or wider than the predetermined width and carrying a clock signal; and

dummy patterns provided in a second wire layer immediately above or below the first wire layer, said dummy patterns being arranged in areas overlapping positions of said second wires and being absent in areas overlapping positions of said third wires.

Claims 14 – 16 (Canceled).

Claim 17 (New): The semiconductor integrated circuit as claimed in claim 8, wherein said square dummy patterns having different sizes are arranged at respective different patter intervals.